# Krishna Savant Syreddy

http://www.sksavant.net
savant@sksavant.net
http://github.com/sksavant
0091-975-703-3532

## EDUCATION

**Indian Institute of Technology (IIT) Bombay** (Mumbai, India)

B.Tech. in Electrical Engineering, *July 2014*

- Control Systems
- Artificial Intelligence
- Machine Learning
- VLSI CAD
- Functional Programming
- Matrix Computations
- Optimization
- Advanced Computing
- Quantum Mechanics

## WORK EXPERIENCE

**Multiview Registration of PointClouds**

Google Summer of Code 2014, Point Cloud Library (PCL), *May 2014 - Jul 2014*

- PCL is an OpenSource 3D Computer Vision processing library.
- The project extends the functionality of pcl::registration by adding algorithms for automatic multiview registration from unordered views.

**Analyzing Point Clouds : Bridge Analysis Project** (Pittsburgh, PA)

Summer Research Scholar, Robotics Institute, CMU, *May 2013 - July 2013*

- The project involved building an application of using an UAV for inspecting bridges. UAV equipped with LIDAR is used to procure laser range data which is then processed into point clouds. Once the point clouds are registered and a model of the bridge is created, it can be visualized from various viewpoints to look for structural deformations. A timelapse of the model is created to observe changes with time.
- I have worked on the registration pipeline using PCL to construct 3D model of the bridge from point cloud data. I have extracted harris keypoints, computed fpfh features at the keypoints, found initial transformation using SAC Initial Alignment and then applied ICP to fine tune alignment. I have implemented metrics to quantify coverage between two point clouds so that a traversal path can be planned given the model.

**Plugin to import and export gEDA/gschem files**

Google Summer of Code 2012, GNUCAP, GNU Project, *May 2012 - Sep 2012*

- GNUCAP stands for GNU Circuit Analysis Program. GNUCAP works with multiple netlist formats such as Spice, Verilog-AMS.
- I have worked on implementing a parser as a dynamically loadable plugin based on a state machine to import circuit schematic files, from gschem and convert them to Verilog-AMS. I have developed a schematic writer to output schematic file from a given Verilog-AMS netlist.

## PROJECTS

**Autonomous Underwater Vehicle Project (AUV-IITB)**

- The project involves designing and developing an AUV that localizes itself and performs realistic missions based on feedback from visual, inertial, acoustic and pressure sensors using thrusters and pneumatic actuators.
- AUVSI Robosub 2013, San Diego, CA. *Sep 2012 to May 2013*
  - We qualified into semi-finals and placed 10th among 30+ teams at Robosub, an underwater robotics competition sponsored by AUVSI and Office of Naval Research and held in San Diego, CA in July 2013.
  - I have worked on software stack of the vehicle which is built using ROS (Robot Operating System). More specifically, I have worked on the navigation system including mission planning and scheduling, path planning and control system of the vehicle. I have implemented a simulator for the vehicle using gazebo, a 3D simulator.
- AUVSI Robosub 2014, San Diego, CA. *Sep 2013 to May 2014*
  - I have led a 6 member software subdivision of the team
  - I have worked on the control system and testing framework of the vehicle

**Spline smoothing of trajectories for robotic arm**, *Oct 2013 - Nov 2013*

- The project involves generating trajectory plans and smoothing them using spline smoothing methods. MoveIt trajectory planner is used for generating trajectories.
- I have implemented and evaluated various spline trajectory smoothing and interpolation methods viz., Cubic spline, Hermite spline, Akima spline and Quartic spline.

**Technology Mapping using Graph covering**, *Oct 2012 - Nov 2012*

- The project addresses the problem of implementing a digital network given a library of gates with the objective of minimizing the cost.
- I have modeled the network and the library components as a DAG. The DAG is then partitioned into forest of trees and each tree is optimally covered by the library.

**epsilon to verilog : A Hardware Compiler**, *Oct 2012 - Nov 2012*

- epsilon-to-verilog synthesizes programs written in a custom minimalistic high level language to hardware description language. It consists of a frontend which outputs Verilog-HDL and a backend which interprets the written program
- I have developed the verilog frontend to output hardware synthesizable code. It works by parsing the control flow graph, scheduling the operations and writing Verilog-HDL output.

## SKILLS

C++, Python, Haskell

Embedded Systems, Microcontrollers, Linux

ROS, OpenCV, PCL

## REFERENCES

- Sebastian Scherer,
  Systems Scientist,
  Robotics Institute, CMU
- Leena Vachhani,
  Professor,
  Systems and Control Engg., IIT Bombay
- Sachin Patkar,
  Professor,
  Electrical Engg., IIT Bombay

## SCHOLASTIC ACHIEVEMENTS

All India Rank 61 in IIT-JEE 2010 of 455,000 students

All India Rank 3 in NEST (National Entrance Screening Test) 2010 of 18000 students

Qualified in Indian National Chemistry Olympiad 2010 and Indian National Physics Olympiad 2010

Awarded Certificate of Merit by Central Board of Secondary Education (CBSE) for being among top 0.1 % in Science and Social Science in 2008